Midterm Exam

(February 16th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

a) Complete the following table. Use the fewest number of bits in each case: (9 pts.)

REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
	11011001		
		0100101	
		1000010	
			101100
			1000000

b) Convert the following decimal numbers to their 2's complement representations. (3 pts.)

✓ -16.1875 ✓ 37.3125

c) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)

✓ -89 + 128 ✓ -61 -13

Problem 2 (18 pts)

- Calculate the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed point number. For the division, use $x = 5$ fractional bits.

1.0001 + 1.001001	1000.0101 - 1.010101	
01.011 × 1.01101	1.001 × 1.0101	01.01110 ÷ 1.011

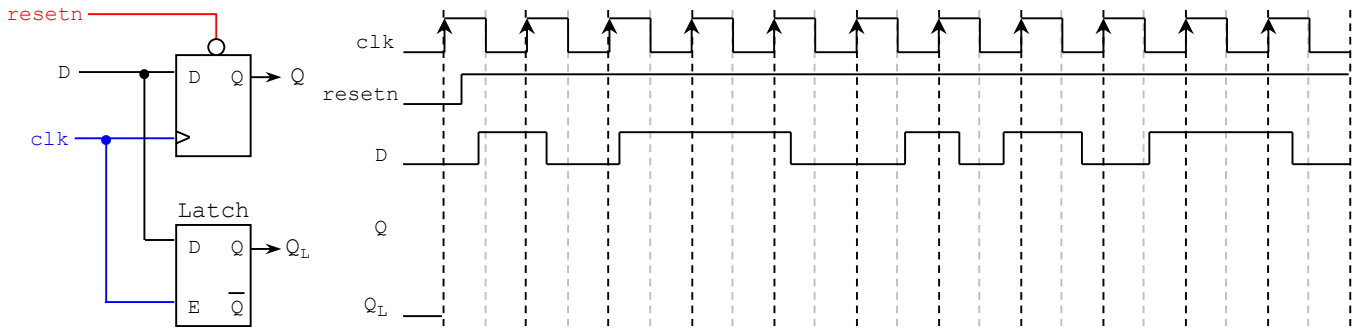
Problem 3 (26 pts)

- Calculate the result (provide the 32-bit result) of the following operations with single floating point numbers. Truncate the results when required. When doing fixed-point division, use $x = 4$ fractional bits.

✓ 40B80000 - 42FA8000	✓ 80123000 + FACE8000	✓ 0A800000 × FAB80000	✓ 7B390000 ÷ C8C00000

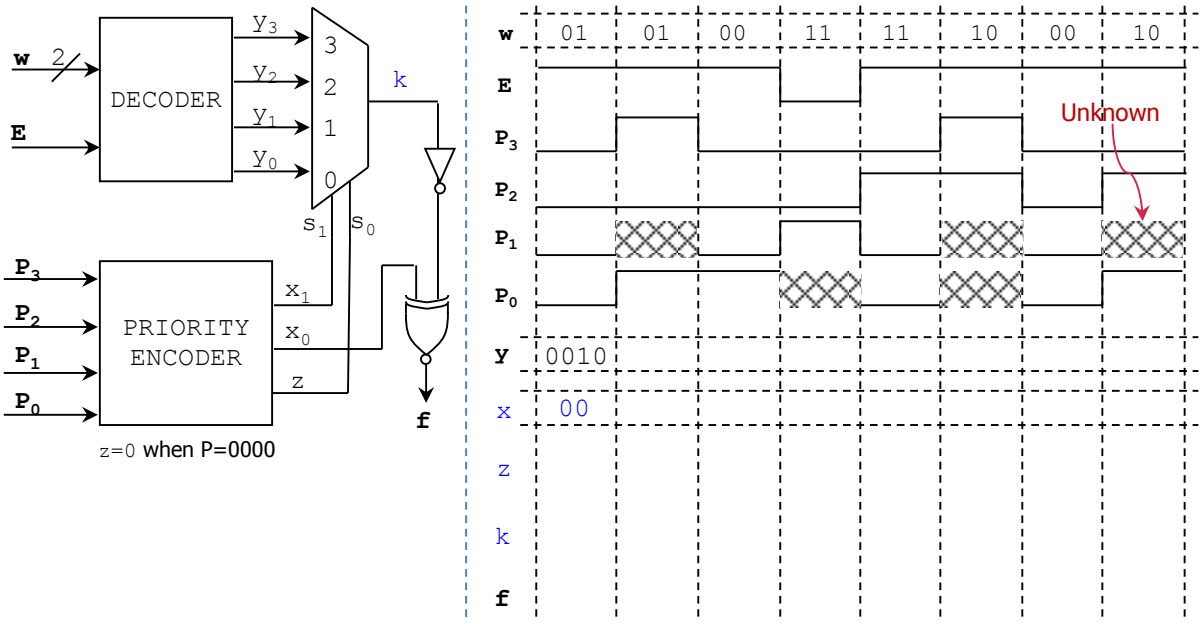
Problem 4 (8 pts)

- Complete the timing diagram of the circuit shown below:



PROBLEM 5 (13 PTS)

- Complete the timing diagram of the circuit shown below. Note that $x = x_1x_0, y = y_3y_2y_1y_0$



PROBLEM 6 (15 PTS)

- The following circuit is a parallel/serial load shift register with enable input. Shifting operation: `s_l=0`. Parallel load: `s_l=1`.
  - ✓ Complete the timing diagram of the circuit: